MuMec: Designing and Building an Improved Hearing Aid

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This document serves as a summary of my non-proprietary research done at MuMec.

Motivation for Improving on Current Hearing Aid Designs

We start with background research on existing hearing aids and current design principles to better understand the market at the moment.

Current Market Trends and Areas of Focus

1. COMPLEX NEW ALGORITHMS: Computational capability (instructions per second, or IPS) needs to increase, as does memory.[1]
2. SMALLER DEVICES: "Invisible" form-factors[2] in the deeper regions of the ear canal require smaller devices.
3. CROSS-DEVICE INTEGRATION: Users want to control their hearing aids with phones or similar devices with little to no hassle
4. FREQUENT FEATURE-SET ROLL-OUTS: As market competitiveness increases, manufacturers need to introduce better algorithms more often, shortening product-life and development cycles.
5. FIELD "UPGRADEABILITY": Upgrades should be deployed live even after the initial purchase to dynamically implement improved feature-sets with the same physical device.
6. RECHARGEABLE BATTERY TECHNOLOGY: Increased user convenience.
7. LOW-COST PERSONAL SOUND AMPLIFICATION PRODUCTS (PSAPS): The same devices that compensate for hearing impairment can be used to amplify other environmental sounds, possibly signaling a paradigm shift that can disrupt the market.
8. IMPROVED BUSINESS MODELS: Direct-to-consumer models can drive component-wise price-reductions and increase price competition.

[1] IPS as a measure of performance can be misleading, since it depends on the specific instructions executed, their order, system clock frequency, and more. There is also no universal benchmark.

[2] IIC (Invisible-In-Canael) tech sits deep in the ear canal for maximum discretion.

Hearing Aid Design Considerations

Given that there is plenty of room for innovation, the current market situation is dynamic; it is likely that going forward, a dramatic change in our approach to hearing-aid design, from product design to consumer-interaction, will change. Specifically, the hardware-specific decisions that need to be made will be governed by these considerations, and 7 other key areas that ON Semiconductor© have identified:

1. GENERAL SYSTEM CHALLENGES:

More basic designs require only processor and memory chips, but others require several for a wireless controller, wireless radio, various sensors, analog front-end, power management, and more. Advanced designs may also require electrostatic discharge (ESD) devices, capacitors, microphones, receivers, antennas, and more. The overall system must satisfy 3 primary objectives:

- Good Performance[3]
- Minimal Power Consumption[4]
- Small Size

[3] measured by sound quality and computational capability

[4] Supply voltage is often around 1.0 V

It is evident that optimizing for one design parameter compromises another. Different specific applications may warrant greater consideration in one of these areas, but overall, balance is necessary and difficult to achieve.

2. DIGITAL SIGNAL PROCESSING (DSP) ARCHITECTURE:

The DSP architecture selected can vary on a spectrum from a closed approach (least customizability and flexiblity) to general-purpose open-programmable approach (most flexible). We consider some variants below:

- *Closed Platform*: Signal processing schemes are hard-coded into the chip, and while a few parameters may be adjustable, most will not be. These are good for highly specific applications leading to lower energy requirements, but are inflexible in the general case.
- *General-Purpose Open-Programmable*: Allow modification of the DSP algorithms, at the cost of increased size and power consumption.[5]. These will typically not satisfy hearing aid performance requirements due to supply voltage and power consumption limitations.
- *Semi-Programmable*: Some programmability enabled, some functionality hardwired in logic blocks. Some additional functionality can be implemented in software but major changes will require a new chip or redesign. Gain some flexibility compared to Closed Platform at cost of some power efficiency.
- *Application-Specific Open-Programmable*: Designed for a very specific application, offering flexibility while mitigating many of the power efficiency concerns of fully open-programmable architectures.[6] This seems to be the optimal balance.

[5] since the chip must be compatible with a range of programmer intentions (sound processing, image processing, sensor data processing, etc.)

[6] Efficient chip-design and apt process-node selection required.

3. CHIP-LEVEL INTEGRATION:

Each chip consists of several individual blocks and components that must work together seamlessly to achieve optimal chip-level integration.

- *Analog Front-End (AFE)*: After microphones convert sound to an analog electrical signal, converts to digital for the processor.
- *Processor*: Performs signal processing; sometimes combined with a separate microprocessor called a DSP or other computing units.

- *Output Stage*: Pulse-width modulation for digital amplification to the receiver.
- *Memory*: RAM, typically integrated on the processor chip, is subject to data loss on power-down. EEPROM[7] is non-volatile and persistent memory storage and therefore stores the DSP fitting parameters and data logs.
- *Power Management*: Optimizes battery usage.
- *User Interface (UI)*: Handle all input/feedback from user (volume, buttons, etc.)
- *Wireless Communication*: Interface the hearing aid with smartphones, other hearing aids, or similar devices.
- *ESD circuitry*: Protect the device.

[7] Electrically-Erasable Programmable Read-Only Memory

Design Partitioning Considerations: The more blocks that are combined on a single die for a chip, the less modular the design becomes. But the fewer blocks there are per-chip, the greater the size. The need to balance these competing constraints drives design decisions. The trend has been towards greater integration, with clever techniques used to reduce integration risks.

4. SEMICONDUCTOR PROCESS:

   Smaller node semiconductor technologies are desirable for decreased power consumption and increased size and speed, but processing difficulties increase greatly. Development costs also increase exponentially for smaller nodes, since more design cycles and testing will be required.

5. STANDARD CPU USAGE IN MULTI-CORE ARCHITECTURES:

   Multi-Core technology enables parallelization and subsequently increased speed. These are necessary due to increased performance requirements and need for wireless functionality. A common misconception that standard cores cannot meet power consumption requirements has led to the design of custom cores. However, sub-micron technologies (smaller transistors) are narrowing the advantages that proprietary cores have, and the use of standard and custom cores in conjunction can enable wireless baseband functionality and power usage optimization. Furthermore, the usage of standard cores reduces development time, prevents duplication of documentation, and allows reliance on more extensive technical support.

6. WIRELESS:

   Wireless communication between hearing aids in a matched pair, or across devices and hearing aids, presents challenges. Smartphones such as iPhones (potentially others, soon) has 2.4 GHz integration enabling direct interfacing of hearing aids to devices. Users can customize the ways in which they interact with their hearing aids.

   - *Near-Field Magnetic Induction (NFMI)*: Range of under 3 feet, requires use of intermediary relay for longer (practical) distances . Bluetooth® has been used to link the relay and audio source.

- *Radio Frequency (RF)*: Much larger range (25 feet) eliminating the need for relays, but requires transmission and receive frequencies to be matched; an adapter can be used to convert the signal to the appropriate frequency.

Convergence on a wireless standard frequency has not been achieved, but might be beneficial. Ultra-low power technologies may also help overcome existing shortcomings if they can offer high data-rates at low power consumption.

7. SYSTEM-LEVEL INTEGRATION:

Chips and electrical considerations form only a part of the entire hearing aid system.

- *Electro-acoustics*: Microphones and Receivers must also be highly reliable and miniature. Sound leakage and vibrations should be minimized.
- *Mechanical Design*: All the components (chips, microphones, transducers, battery, PCBS, buttons) need to be optimally placed in the final package.

These factors must be optimized (keeping system flexibility in mind) to ensure that the overall performance, power consumption and size objectives are met. New methods for packaging electronic components may emerge as well.[8]

[8] For example, consider integrated passive device (IPD) techniques and vertical connection techniques such as through-silicon vias (TSVs). These reduce signal distances and improve electrical performance.