160 µW, High-Slew Smartwatch LCD Driver

EE 140 Final Project Presentation

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Summary

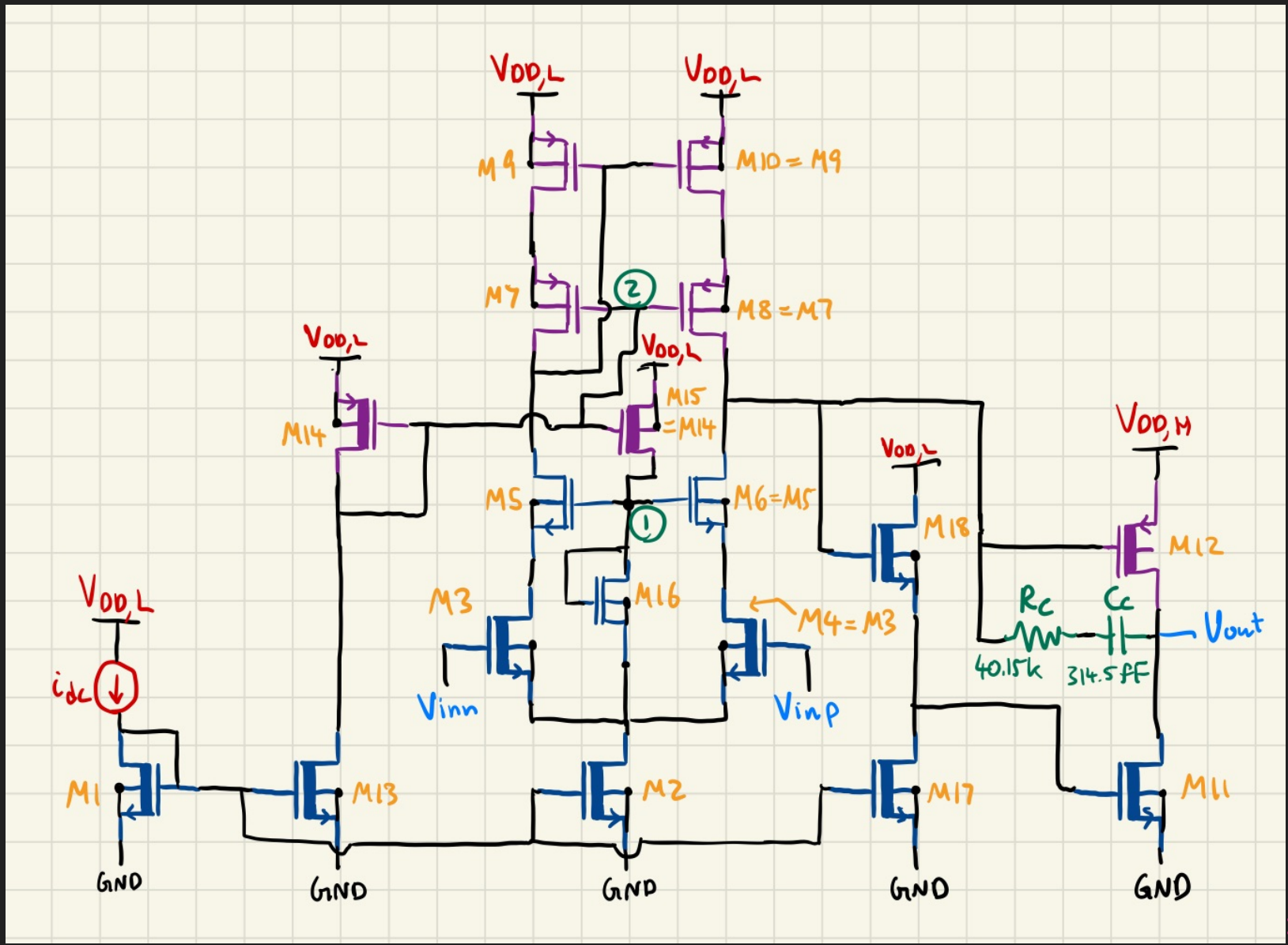
Introduction

Comparison with Target Specifications

Property	Specification	Achieved
Power Supplies	≤ 1.8V, GND	1.8V, 1.62V, GND
Closed Loop DC Gain	2	2
Load	800Ω, 30pF	same
Max. Settling Time	180.22ns	178.57ns
Total Error	0.2%	0.013%
Power Consumption	$\leq 750\mu$W	159.24μW
Output Voltage Swing	≥ 1.4	≥ 1.4
Max. Mirror Ratio	20	18
Max. Added Capacitance	25pF	75fF
CMRR at DC	≥ 60dB	87.03dB
PSRR at DC	≥ 50dB	59.498dB
Phase Margin	$\geq 45^\circ$	56.16°
FOM	≥ 7.403	35.17

Motivation for Choosing Topologies

Diagram of Circuit (values have since changed)



Stage 1 Considerations

1. **High Gain**; meet static error and allow greater proportion of 0.2% to go to dynamic, transient error.
2. **Slew Rate**: current drives a small capacitance (compensation) and stage has a somewhat small output swing (second stage applies gain to signal).
3. Standard Differential Amplifier doesn't provide enough gain; *need to cascode* $\implies$ telescopic cascode is a valid option.

Stage 2 Considerations

1. **Large Output swing**; ensure $V_{\text{ds,sat}}$ of devices isn't greater than 200mV.
2. **Slew Rate**; Driving large (30pF) load (and also smaller compensation capacitor); need enough current to do so.
3. *gain isn't as significant* (if first stage is designed well).

Compensation

1. **Transient**: with more compensation (higher C, higher R), generally, stage 1 performs worse but stage 2 performs better (but can tune to benefit both!). Amount of compensation determined by which stage is failing the settling time.
2. **Phase Margin**: miller RC compensation (which I used) can improve phase margin and increase unity-gain frequency (bandwidth).

Design Approach and Techniques

Stage 1: Sizing Devices

1. Extensive Matlab $\frac{g_m}{I_D}$ analysis to find the point of maximizing *gain per unit current*.
2. System-level analysis yielded range of viable/optimal g_{m1}, r_{o1} values to aim for. Initially, I constrained myself to precise values; later, relaxed constraints to form bias $\pm$ threshold.
3. Higher values of $\frac{g_m}{I_D}$ selected (but not so high that J_D drops precipitously, requiring very large W).

Stage 1: Biasing

1. Used current mirror network with low current ($2\mu A$) to set up DC node voltages for NMOS/PMOS sides of cascode. Inspired by homework problem.
2. Matlab `look_up` function for a given set of device parameters is more accurate with raw V_{GS}, V_{DS} values than for arbitrary cross-ratios (such as $\frac{g_{ds}}{I_D}$ given a specific $\frac{g_m}{I_D}$).
3. Alter bias voltages as needed to make g_{ds} as similar as possible in a given cascode stack ($8\mu S, 8\mu S$ better than $11\mu S, 5\mu S$).

Stage 1: Impacts of Variables

1. Higher length leads to minimal change in power consumption, large increase in gain, and slower settling response.
   - But, can tune to ideal state where improvement in static error outweighs generally slower settling response (for me, 480nm).
2. Input common-mode voltage: minimum; large enough to keep devices in saturation, optimal; make g_{ds} of input devices collectively low.
3. Use widths to control $V_{\text{ds, sat}}$ (pick devices where g_m value matters less, like top stage 1 PMOS devices).

Stage 2: Sizing Devices

1. Matlab analysis yet again (started with class A common source, which was very similar to labs).
2. Matlab "optimal" sizes would often lead to output bias voltage $\neq 900$mV; needed to tune widths in Cadence. Sometimes had to compromise; tuning PMOS $\implies$ different $g_{m,p}$ than planned. tuning NMOS $\implies$ different bias current than planned (for class A).

Stage 2: Current/Length Selection

1. Selected length based on system-level estimate for f_U (larger lengths may violate unity-gain frequency requirement). Higher lengths led to higher gain.
2. Class A Common Source output stage: $g_{m,n}$ doesn't impact performance much (NMOS is there to set a branch bias current). Class AB stage: $g_{\text{m,eff}} = g_{m,n} + g_{m,p}$ (two signal paths) so both devices matter.
3. Wider devices consume more power (more current). Want minimally sized widths that provide enough current to settle within 180ns.

Stage 2: Why a Source-Follower?

1. Effective DC level-shifter
2. Simple to bias and integrate into a class A common source approach (which I had before). Can bias with generally low current ($\leq 3\mu A$), and use relative widths to set V_{GS} of NMOS device.
3. Overcome slew-rate limit that makes class A very power-hungry + take advantage of increased $g_{m,eff}$.

Compensation

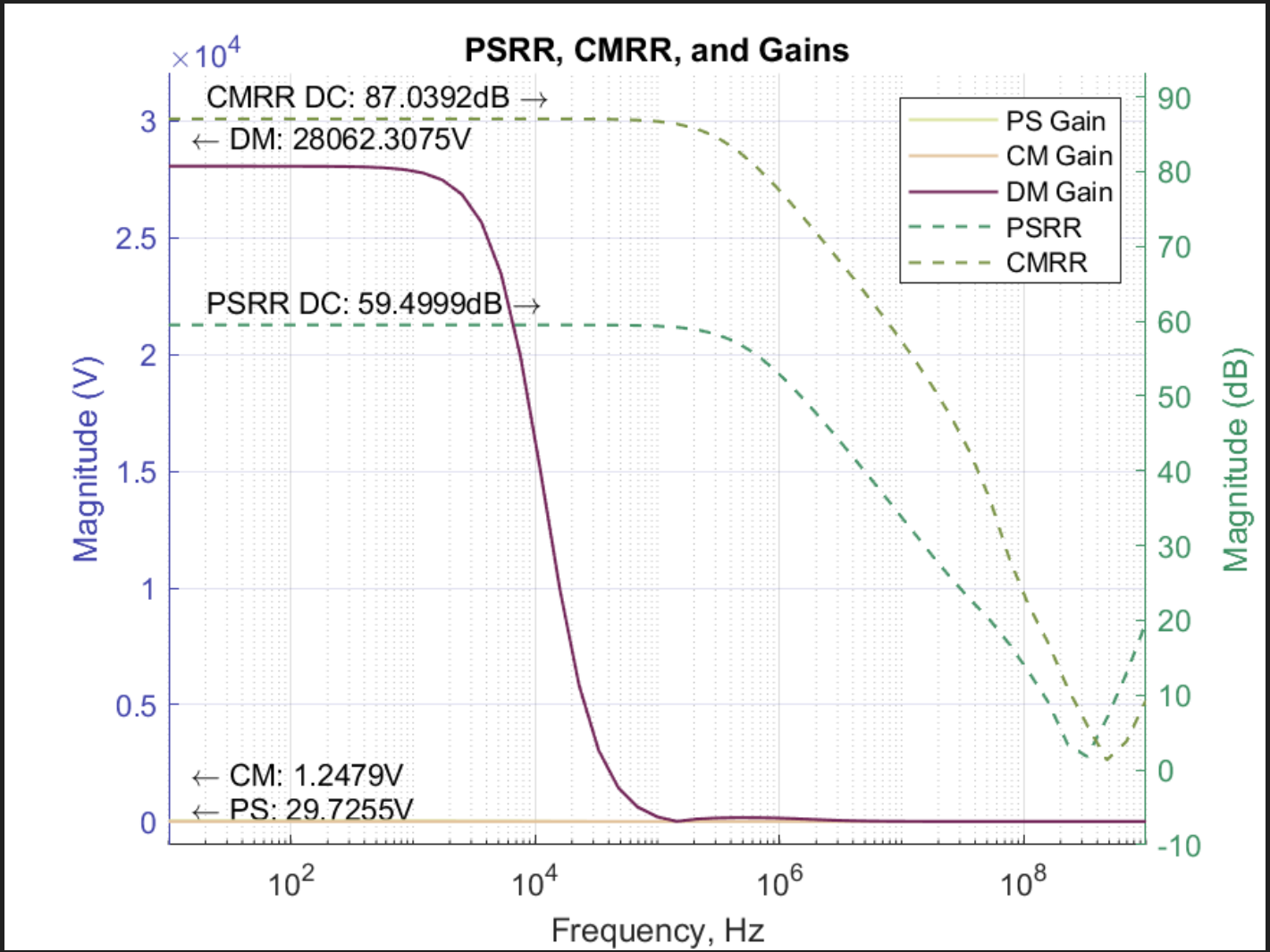
1. Matlab can't predict slew-rate limitations; led to more reliance on Cadence testing and parameterized sweeps.
2. For a given design, once the DC bias points were tuned, then I honed in on the optimal compensation with 3-4 parametric analyses on C_C, R_C.
3. These had minimal impact on power ($\leq 1\mu W$), didn't change bias points (compensation tuning done last for any given design).
   - In later stages of project, testing the response of a candidate design at a few compensation levels would indicate quickly if the approach was worth pursuing or not (to meet setting time).

Some Other Thoughts

1. Optimizing for power is far more rewarding (FOM-wise) than optimizing for settling time. My Matlab analysis indicated that approximate optimal settling time is $85 - 90$ns, only half of 180ns (and requires massive power).
2. Matlab matches Cadence only to an extent (especially transient response).

Performance Verification

Plot of Values

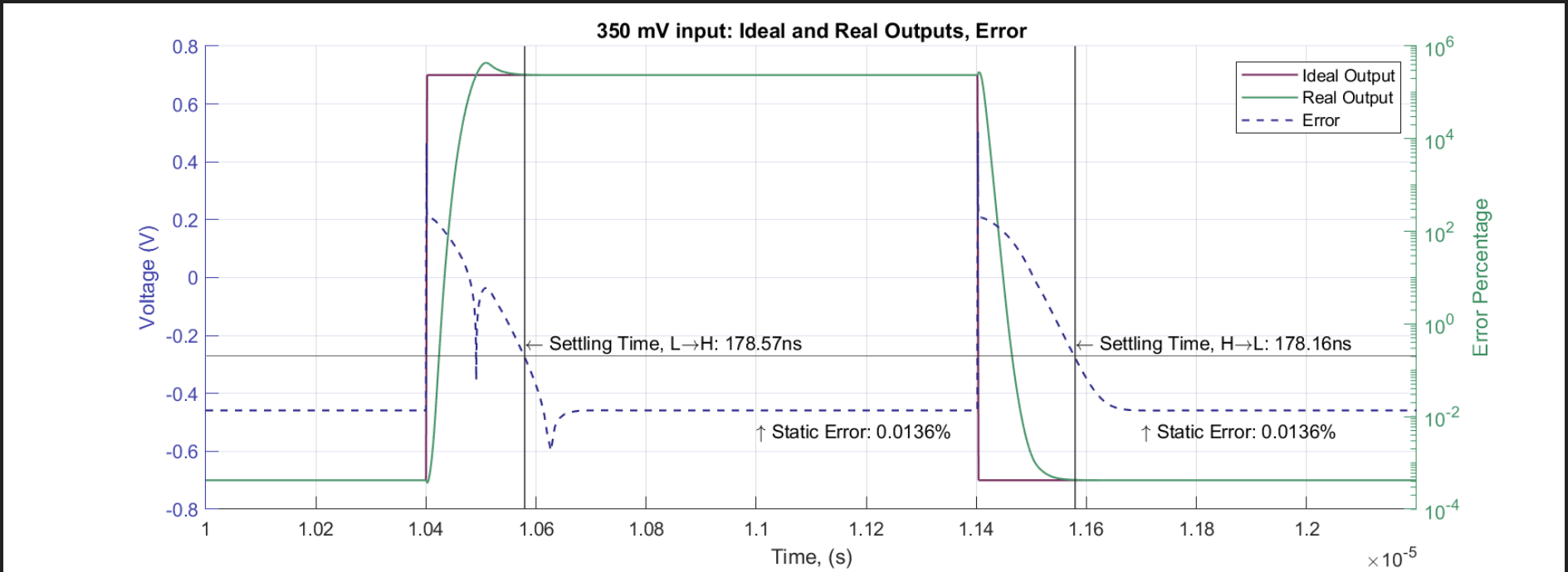


ADE Output (Confirmation of Plot Values)

Outputs

	Name/Signal/Expr	Value	Plot
1	cm_gain	wave	☑
2	dm_gain	wave	☑
3	CMRR	87.0356	☑
4	CMRR_freq	wave	☑
5	ps_gain	wave	☑
6	PSRR_freq	wave	☑
7	PSRR	59.4983	☑
8	Phase Margin	56.1613	☑
9	Phase Margin Frequency	31.1979M	☑
10	Loop Gain Phase	wave	☑
11	Loop Gain dB20	wave	☑
12	Output Bias Voltage	900m	☑
13	I9/Vmid		☐
14	I9/Vup		☐

Plot of Response (350mV)



Analyzing Step Response (350mV)

1. Overshoot in $L \rightarrow H$ is result of too much compensation (but it's needed for $H \rightarrow L$.
2. Linear decrease in $H \rightarrow L$ can be improved with more compensation (evidently, competing with other transition).

ADE Output (Confirmation of Power, Output Swing)

Outputs

	Name/Signal/Expr	Value	Plot
1	vreset		☐
2	vout_low2high	1.40119	☐
3	vout_low_180n	201.288m	☐
4	vout_low	200.11m	☐
5	vout_load	wave	☐
6	vout_int		☐
7	vout_high2low	1.39863	☐
8	vout_high_180n	1.6013	☐
9	vout_high	1.59992	☐
10	vout		☐
11	vin_n		☐
12	vin	wave	☐
13	settling_error_low2high	-84.7324m	☑
14	settling_error_high2low	97.7218m	☑
15	iavg_1	-26.7447u	☑
16	power_1	-43.3265u	☑
17	iavg_1p8	-64.3957u	☑
18	power_1p8	-115.912u	☑

Plot of Response (5mV)

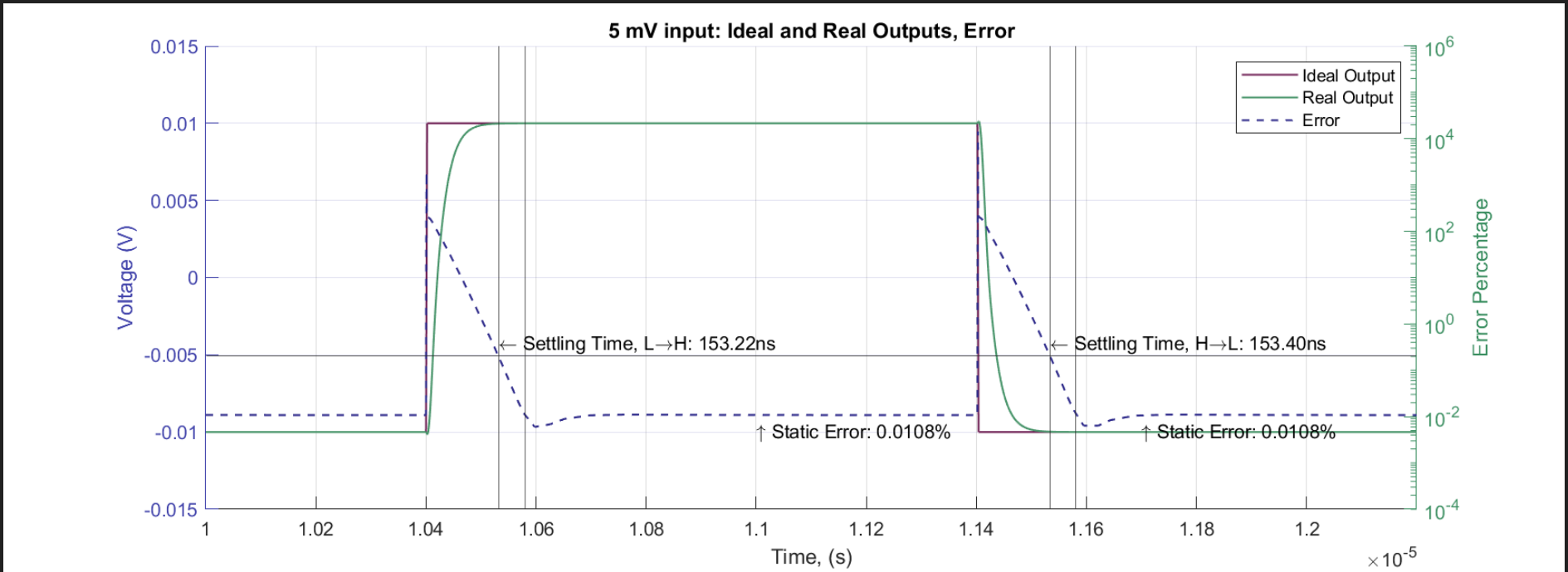


Figure of Merit Calculation

$$\begin{aligned}\texttt{FOM} &= \frac{10^{-9}}{t_{\text{settle}} \cdot P_{\text{tot}}} \\ &= \frac{10^{-9}}{178.57\text{ns} \cdot 159.24\mu\text{W}} \\ &= 35.167\end{aligned}$$

Full Changelog (important ones bolded)

Result of Changes (made since submission of report): FOM increased from 26.09 to 35.17.

1. **Decrease Stage 1 Current** (less power)
2. **Increase Stage 1 lengths** (higher gain, lower static error allowed higher dynamic error)
3. Tune bias voltages using mirror-network parameters.
4. **Decrease stage 2 length** (increase power consumption but improve transient response)
5. Decrease compensation to account for other changes.

Possible Points of Optimization

1. Individualized NMOS input vs NMOS vs PMOS Stage 1 lengths (mostly same now).
2. Replace compensation resistor with triode transistor (for area + PVT matching).
3. Improved class AB implementation (current injector? IEEE Hogervorst paper? Mehta's Improved Hogervorst design from JSSC '19?)
4. Explore cascode compensation
5. Decrease bias currents more.

Acknowledgments

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The End! Questions?