Neelesh Ramachandran

www.neeleshramachandran.com | (408)-642-4720 | neeleshr@stanford.edu | linkedin.com/in/neelesh-ramachandran

EDUCATION

Stanford University: M.S. Electrical Engineering **Expected Graduation: May 2024**

Planned Coursework: Fiber Optic Comm. (EE 247), Fourier Transform Applications (EE 261), Applied Quantum Mechanics (EE 222)

University of California, Berkeley: College of Engineering **Expected Graduation: May 2022**

B.S. Electrical Engineering & Computer Sciences (EECS) GPA: 3.97

Selected Coursework (* for A+ grade): Mixed-Signal Chip Tapeout (*EE 194*)*, Analog IC Design (*EE 240B*, EE 140, EE 105**), Digital IC Design (*EECS 151*)*, Probability (*EECS 126*), Control Systems (*EE C128*), Quantum Mechanics (*Physics 137A*), Optimization (*EECS 127*), OS Programming (*CS 162*), IC Device Physics (*EE 130*)*, Computer Architecture (*CS 61C*)*, Optical Engineering (*EE 118*)*

WORK EXPERIENCE

Apple / *Wireless Platform Architecture Intern (12 weeks)* May 2022 – August 2022

- Delivered a C++ library to integrate a C++ wireless network simulation engine with Python machine learning frameworks, using ZeroMQ (brokerless client-server messaging). Enabled efficient and robust real-time info transfer between programs.
- Enhanced large file storage (LFS) organization and scripting to reduce storage space by 88% and repo operation times by 95%.
- Learned Modern C++ (14, 17), implemented neural-network classifiers in Python, studied details of Git, Stash, Bitbucket LFS

Apple / *Power Manager (PMGR) Design Verification Intern (15 weeks)* May 2021 – August 2021

- Implemented extensive automation (>50x time-savings) with from-scratch Python3, YAML/JSON scripting infrastructure.
- Revamped a chip-level testbench to decrease build- and run-times by over 85% (System Verilog, UVM, functional coverage).

MuMec Inc. / *Electrical Engineering Intern (Project Lead) (11 weeks)* May 2021 – August 2020

- Built and programmed a functional hearing aid from-scratch, with custom firmware and DSP algorithms.
- Designed impedance matching network to optimize RF signal strength, validated the core chipset using test equipment.
- Performed precision hand-soldering (0402 components) and learned reflow soldering for 0201 components.

6-semester TA/uGSI for Devices & Systems I and II (EECS 16A/B) / *Content, Discussion, Software* August 2019 – May 2022

- Developed ~150 pages of notes, wrote 8 discussion worksheets, taught recorded sections viewed by 700+ students in Spring '21.
- Independently authored a ~130 page textbook with content and practice problems + solutions. ~55k visits since Summer '20.
- Education research: writing algorithms to intelligently form student study-groups from survey responses for remote learning

CLUB / PROJECT EXPERIENCE

Mixed Signal Chip Tapeout / Analog Front-End Baseband Block January 2022 – May 2022

- Designed, tested, and fully layed-out the baseband block of the chip's radio front-end (FinFET technology, 22nm)
- Variable Gain Amplifier: 2-stage core op-amp (folded-cascode) with common-mode feedback circuit, common-centroid layout
- Bandpass Filter: Multiple-feedback active filter design, dynamic center-frequency tunability using Cap DACs
- Current DAC for DC offset cancellation, Transimpedance Amp., Resistor and Capacitor DACs for tuning

Berkeley Formula Racing (FSAE) / *Electrical Subsystem Co-Lead* August 2018 – May 2020

- Designed custom PCBs (brake thermocouple board, combined accelerometer/gyroscope board, and others).
- Optimized routing and manufacturing of 3 modular wire harnesses (ECU (engine), ADL (sensors), Power).
- Developed live telemetry, shifting-lights PCB, ECU/ADL Validity Checker, automated wire-routing, and others.

UC Berkeley IEEE Student Branch / *Director of Professional Development* August 2018 – December 2019

- Organized events such as Resume Workshops, Graduate Research Mixers, Interview Workshops, and more.

RESEARCH EXPERIENCE

LEED Lab / *Undergraduate Student Researcher* August 2020 – Present

- Designed a next-generation memory (FDSOI) transistor exploiting memory of a ferroelectric layer (Sentaurus, TCAD).
- Published in the IEEE journal for Transactions on Electron Devices ("Dynamical Effects of Excess Carriers On SOI FeFET Memory Device Operations"). Accepted in Sept. 2022, journal issue pending.
- Simulated ferroelectric gate layers for increased hysteresis (memory window) and efficient transistor read/write operations.
- Investigated carrier dynamics to minimize read delay, optimizing endurance and read margin.

SKILLS

Hardware: Analog Circuit Design, RF Circuits, Schematic Capture, Device Design, TCAD, Spice, Prototype, PCB Design & Manufacturing, Chip/Board Testing, Verilog / System Verilog, FPGA, UVM, Functional Coverage, Code Coverage, Precision Soldering

Software: Python, Java, C, C++, Perl, RISC-V, Matlab, Data Structures, Algorithms, Operating Systems, Data Analysis, Debugging (GDB)

Other: LaTeX, Git, Technical Writing, Applied Research, Teaching, Mathematica